REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-7, 9-11, 14-34, 36-38, 41-54 and 58-60 are presently active. Claims 55-57 and 61 were previously cancelled. Claims 8, 12-13, 35, and 39-40 have been presently cancelled without prejudice or disclaimer. Claims 1, 28, and 58 have been presently amended. No new matter has been added.

Applicant acknowledges with appreciation the consideration of this matter and the related appeals in U.S. Serial Nos. 10/673,138, 10/673,501; 10/673,506; and 10/673,583 by the Board.

Claim 1 as clarified defines:

> 1. A method of controlling a process performed by a semiconductor processing tool, comprising:
> inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;
> inputting process data related to an actual process being performed by the semiconductor processing tool;
> setting initial and boundary conditions ***for a spatially resolved model of a physical geometry of the semiconductor processing tool*** based on said process data related to the actual process being performed by the semiconductor processing tool;
> solving the computer-encoded differential equations of the first principles simulation model ***for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed***;
> providing a first principles simulation result from the solution of the computer-encoded differential equations solved concurrently with the actual process being performed; and
> using the first principles simulation result obtained during performance of the actual process to build an empirical model; and
> selecting at least one of the first principles simulation result and the empirical model to control the actual process being performed by the semiconductor processing tool. [Emphasis added.]

Applicant's specification at numbered paragraph [0035] states:

> Thus, the first principles physical model 106 depends to some extent on the type of semiconductor processing tool 102 analyzed as well as the process performed in the tool. For example, ***the physical model 106 may include a spatially resolved model of the physical geometry of the tool 102***, which is different, for example, for a chemical vapor deposition (CVD) chamber and a diffusion furnace. Similarly, the first principles equations necessary to compute flow fields are quite different than those necessary to compute temperature fields. The ***physical model 106 may be a model as implemented in commercially available software, such as ANSYS, of ANSYS Inc., Southpointe, 275 Technology Drive Canonsburg, PA 15317, FLUENT, of Fluent Inc., 10 Cavendish Ct. Centerra Park, Lebanon, NH 03766, or CFD-ACE+, of CFD Research Corp., 215 Wynn Dr., Huntsville, AL 35805, to compute flow fields, electro-magnetic fields, temperature fields, chemistry, surface chemistry (i.e. etch surface chemistry or deposition surface chemistry)***.

One of ordinary skill in the art would know that a "spatially resolved model of a physical geometry of the semiconductor processing tool" is simply a model of the physical geometry of the tool using separated points in space.

Applicant's specification at numbered paragraph [0091] describes a number of process sensors detecting for example mass flow rates, chamber pressure, temperatures of the substrate holder and the substrate, a temperature of a backside gas coolant, gas gap pressure, and vacuum pump inlet pressure. Thereafter, Applicant's specification at numbered paragraph [0092] states:

> A diagnostic controller **1324** can be coupled to each of the ***sensors*** described above ***and can be configured to provide measurements from these sensors to the simulation module described above***. For the exemplary system of FIG. 13, the model executed on the simulation module can, for example, include three components, namely, a thermal component, a gas dynamic component, and a chemistry component. In the first component, the gas-gap pressure field can be determined, followed by a calculation of the gas-gap thermal conductance. Thereafter, the ***spatially resolved temperature field*** for the substrate (and substrate holder) can be determined by ***properly setting boundary conditions (and internal conditions)*** such as ***boundary temperature, or boundary heat flux, power deposited in resistance heating elements, power removed in cooling elements, heat flux at substrate surface due to the presence of plasma,*** etc. [Emphasis added]

Applicant's specification at numbered paragraph [0057], states:

> In this embodiment, steady-state simulations are repeatedly run concurrently with the process by using the physical sensor measurements to repeatedly update boundary conditions of the first principles simulation model.

Hence, Applicant discloses 1) a physical model 106 including a spatially resolved model of the physical geometry of the tool 102, 2) physical model 106 implemented in commercially available software such as ANSYS or FLUENT to solve a spatially resolved model, 3) the setting of boundary and internal conditions, 4) repeated running of simulations concurrently with the process, and 5) using physical sensor measurements to repeatedly update boundary conditions of the first principles simulation model.

The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." United States v. Telectronics, Inc., 857 F.2d 778, 785 (Fed. Cir. 1988).

For the Examiner's consideration of what was known in the art at the time of filing,[1] attached is a 2002 article from *Chemical Engineering Science* entitled: "Visualization and numerical simulation of fine particle transport in a low-pressure parallel plate chemical vapor deposition reactor." This article on page 509 shows the use of spatially resolved model of the physical geometry of a parallel plate CVD reactor (i.e., set of 2,000,000 triangular/tetrahedral meshes). This article on page 499 indicates that the numerical simulations were performed using the commercially available CFD code Fluent 5.3 (Fluent, Inc.). Excerpts from this paper are reproduced below on the next page. While provided for the sake of showing that one of ordinary skill in the art would not have to use undue experimentation to make a spatially resolved model of a physical geometry of the semiconductor processing tool, this reference also does not show the use of solutions from such models being used for process

[1] M.P.E.P. § 2164.05(a), the specification need not disclose what is well known to those skilled in the art and preferably omits that which is well known to those skilled and already available to the public.

control or being produced in a time frame consistent with that of a semiconductor manufacturing process.

Hence, given this knowledge in the art at the time of the invention, Applicants' description of "setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool" does not require undue experimentation and is enabled.

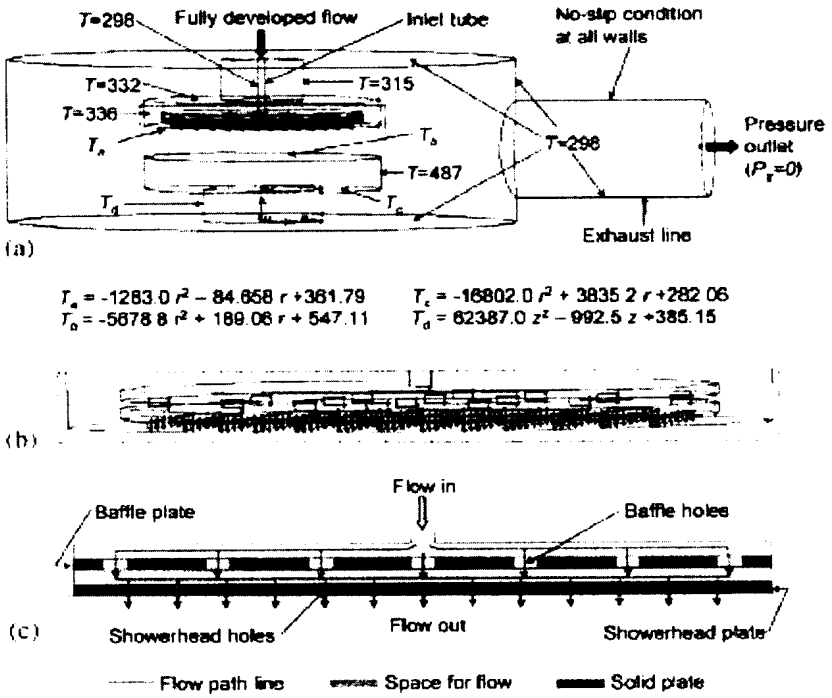


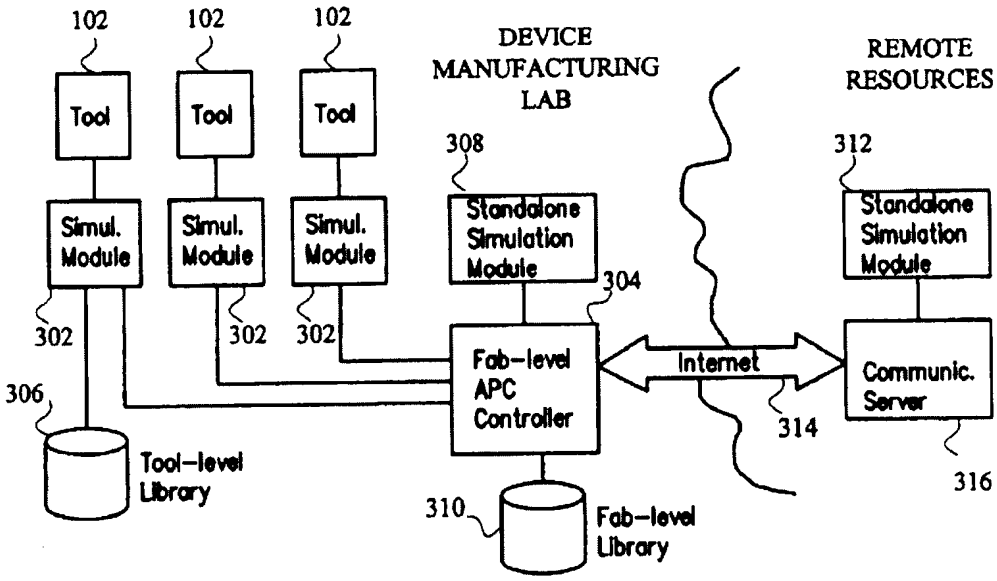
Fig. 3. (a) Computational domain and boundary conditions for the numerical simulation, (b) enlarged picture of the showerhead structure shown in (a), and (c) detail of the showerhead structure. The unit of temperature T shown in this figure is in K. r and z in the fitting equations of temperature profile represent radial and axial positions in m, respectively.

Fig. 4. Unstructured triangular/tetrahedral grid arrangement used in the calculation.

Moreover, "solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed," is enabled as noted in the previously filed Appeal Brief:

> The examiner requested details of the models which lead to the unexpected result of being able to avoid the lengthy time conventionally required for the generation of a first principles model simulation. See page 10 of the Office Action. Appellant points out procedures by which the unexpected results of the invention are achieved. It is not the details of the models, but rather the details as to how the model calculations are implemented which reduce the time for calculations. For instance, the disclosed characteristics in the specification which permit simulation results to be obtained in a time frame compatible with using the first principles model simulation result for real time process control are enumerated below with reference to the numbered paragraphs in the filed specification:
>
> > **1)** the use of interconnected resources inside a semiconductor device manufacturing facility to perform the first principles simulation (see specification, numbered paragraph [0043] and Figure 3, both reproduced below),
> >
> > **2)** the use of code parallelization among interconnected computational resources inside the semiconductor device manufacturing facility (see specification, numbered paragraphs [0047] and [0048] reproduced below),
> >
> > **3)** the sharing of simulation information among interconnected resources inside the semiconductor device manufacturing facility (see specification, numbered paragraphs [0047] and [0048] reproduced below), and
> >
> > **4)** the reduction in redundant execution of substantially similar first principles simulations by the reuse of known solutions as initial conditions for the first principles simulation, as features which used singularly or in combination lead to a simulation result in a time frame consistent with real time process control in a semiconductor processing tool (see specification, numbered paragraphs [0047] and [0048] reproduced below).

Figure 3



[0043] FIG. 3 is a block diagram of a network architecture that may be used to provide first principles simulation techniques to facilitate a process performed by a semiconductor processing tool in accordance with an embodiment of the present invention. As seen in this figure, the network architecture includes a device manufacturing fab connected to remote resources via the Internet 314. The device manufacturing fab includes a plurality of semiconductor processing tools 102 connected to respective simulation modules 302. As described with respect to FIG. 1, each semiconductor processing tool 102 is a tool for performing a process related to manufacturing a semiconductor device such as an integrated circuit. Each simulation module 302 is a computer, workstation, or other processing device capable of executing first principles simulation techniques to facilitate a process performed by a semiconductor processing tool 102. Thus, each simulation module 302 includes the first principles physical model 106 and the first principles simulation processor 108 described with respect to FIG. 1, as well as any other hardware and/or software that may be helpful for executing first principles simulations. Moreover, simulation modules 302 are configured to communicate with the fab-level advanced process control (APC) controller using any known network communication protocol. Each simulation module 302 may be implemented as a general purpose computer such as the computer system 1401 of FIG. 14.

> **[0047]** The present inventors have discovered that the network configuration of FIG. 3 provides computational and storage resource sharing that allows a broad range of first principles simulation results at reasonable solution speeds, thus providing meaningful on-tool simulation capabilities that can facilitate processes performed by the tool. Specifically, while simple simulations may be executed by a tool's dedicated simulation module, complex simulations requiring greater computational resources may be executed using code parallelization techniques on multiple simulation modules in the network that may be on-tool or standalone. Even on-tool simulation modules in equipment currently under preventive maintenance may be used as a shared computational resource, provided there is power to the simulation module. Similarly, simulation results used for later lookup can be stored in libraries (e.g. storage devices) anywhere in the fab network, and accessed by all tools when lookups of diagnostic or control data are made.
>
> **[0048]** The present inventors have also discovered that the network architecture of FIG. 3 provides the ability to distribute model results done at one processing tool 102 for one condition set, to other similar or identical tools operating later under the same or similar conditions, so redundant simulations are eliminated. Running simulations only for unique processing conditions at on-tool and standalone modules and re-using results from similar tools that have already known simulated solutions allows for rapid development of lookup libraries containing results that can be used for diagnostics and control over a large range of processing conditions. Further, the reuse of the known solutions as initial conditions for first principles simulation reduces the computational requirements and facilitates the production of simulated solutions in a time frame consistent with on-line control. Similarly, the network architecture of FIG. 3 also provides the ability to propagate changes and refinements made to physical models and model input parameters from one simulation module to others in the network. For example, if during process runs and parallel executions of a model it is determined that some input parameters need to be changed, then these changes can be propagated to all other simulation modules and tools via the network.

Hence, the examiner should now understand as before (when the former 112, first paragraph, rejections were removed based on this information) that it is the combination of one or more of the network architecture of FIG. 3, the sharing of model results done for one

condition set to other similar or identical tools operating later under the same or similar conditions, the reuse of prior solutions of proven convergence, the reuse of the known solutions as initial conditions for first principles simulation, etc. and **not the details of the model itself** which enable the invention to solve the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed.

These capabilities taught by Applicant's specification permits for the remarkable control of semiconductor manufacturing processes using real time simulation results to control the process.

For example, the examiner will appreciate that, for the parallel plate reactor of Figure 13, a spatially resolved model of the parallel plate reactor and substrate on a stage opposing a plasma heat flux can be provided with the commercially available software, such as ANSYS or FLUENT packages discussed above. The disclosed sensors at numbered paragraph [0091] can provide temperature data of the substrate holder, the substrate, and the backside gas coolant during the process. This process data along with the above-noted properly set "boundary conditions (and internal conditions) such as boundary temperature, or boundary heat flux, power deposited in resistance heating elements, power removed in cooling elements, heat flux at substrate surface due to the presence of plasma, etc." can be used to set the initial and/or boundary conditions of the spatially resolved model.

The simulation then provides for example a spatial mapping of the heat flux to the substrate by taking into consideration heat flux from the plasma to other surfaces of the parallel plate reactor besides the substrate. The spatial mapping of the heat flux to the substrate becomes a simulation result, which can then be used to control the parallel plate reactor.

If the spatial map shows deviations outside the desired uniformity, then the process pressure or the gas composition could be changed while the process is running. With the invention having the capability to solve the computer-encoded differential equations of the first principles simulation model for the spatially resolved model in a time frame shorter in time than the actual process being performed, this simulation tool can simulate the effects of pressure and gas composition changes before actually having to implement the change.

This results in a remarkable advance in process control.

Regarding the art of record, Applicants submit that this rejection should be removed for the following reasons.

Firstly, Claim 1 as clarified recites:

> setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool based on said process data related to the actual process being performed by the semiconductor processing tool.

M.P.E.P. § 2142.02 indicates that:

> In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious.

The art of record in this application or the related appealed applications noted above neither individually nor in combination discloses or suggests setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

The examiner in related application U.S. Serial No. 10/673,507 relied on col. 7, lines 21-35, of Sonderman et al for an asserted teaching of setting initial and boundary conditions

for a spatially resolved model of a physical geometry of the semiconductor processing tool.

Yet, col. 7, lines 21-35, of Sonderman et al merely describes:

> Turning now to FIG. 5, a flowchart representation of the steps for performing the process simulation function described in block 440 of FIG. 4 , is illustrated. The system 100 prepares one or more process models for simulation (block 510). The models that are prepared for simulation may include the device physics model 310, the process model 320, and the equipment model 330. The number of models defined by the system 100 generally depends upon the interactions of model-components that are to be examined by the simulator 340. In other words, the system 100 determines which components in a model are to be modified and which components are to be monitored for reactions caused by the original component modification. One embodiment of a flowchart depiction of the steps of preparing the processing models for simulation is illustrated in FIG. 6

There is no detail here of a spatially resolved model of a physical geometry of the semiconductor processing tool or the setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

The greatest detail of the equipment model provided by Sonderman et al is at col. 5, lines 62-67, which states:

> The equipment model 330 comprises components that can model furnace behavior during semiconductor manufacturing processes. The equipment model 330 can also model the temperature response, pressure response, and at other such characteristics relating to equipment that performs manufacturing processing.

There is once again no detail here of a spatially resolved model of a physical geometry of the semiconductor processing tool or the setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

Moreover, statistical models, like Sonderman et al (and Tan et al), do **not** have initial and boundary conditions, but rather are models which simply correlate inputs and outputs of a process based on statistical data from previous process runs. These models also do not solve for a variable over a gridded spatial domain, but instead use statistics to provide predictions about the end result that would be obtained if a process were run in a certain manner.

Indeed, the one model described in detail in Sonderman et al is their device physics model, which is set forth at col. 9 of Sonderman et al. This "model" is based on performance factors X_{Ai} fed back into line 805, through which a learned model is developed based on the system performance over time. Col. 9, lines 1-11, state:

> Turning now to FIG. 8 , a simplified process control system block diagram is illustrated. The controller 810 controls a process 820 that is performed on a silicon wafer. The input to the controller on a line 805 , is denoted by the term $X_{Ti,}$ which represents a target performance of the processed semiconductor wafer (S_i). Once a particular silicon wafer, S_i, is processed, metrology results 830 will define the actual performance of the processed semiconductor wafer S_i, which is denoted by the term X_{Ai}. The actual performance factor, X_{Ai} is ***fed back*** into the line 805 which is sent to the controller for further adjustments.

Sonderman et al further describe at col. 9, lines 33-40, how the percentage effectiveness (i.e., a statistical metric) is derived based on a multi-variant function (i.e.., another statistical metric).

Hence, the statistical models in Sonderman et al would be of no consequence to initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

Furthermore, while the examiner in related application U.S. Serial No. 10/673,507 relied on col. 3, lines 50-67, and col. 7, lines 8-20 of Sonderman et al for an asserted teaching of inputting process data for an actual process being performed by the semiconductor processing tool, those section of Sonderman et al only state:

> **Col. 3, lines 50-57:** Semiconductor devices are processed in a manufacturing environment using a number of input control parameters. Turning now to FIG. 1, a system 100 in accordance with one embodiment of the present invention is illustrated. The system 100 comprises a process control environment 180, a manufacturing/processing environment 170, and a simulation environment 210. The process control environment 180 controls the operations of the manufacturing environment 170. In one embodiment, the process control environment comprises an APC framework. ***The process control environment 180 can receive data from the manufacturing environment 170 and the simulation environment 210*** and make appropriate

> changes to manufacturing control parameters to affect the operations of the manufacturing environment 170.
>
> In one embodiment, semiconductor devices 105, such as semiconductor wafers, are processed on processing tools 120a, 120b using a plurality of control input signals, or manufacturing parameters, on a line 123.

> **Col. 7, lines 8-20:** Once the system 100 validates the defined models, the system 100 acquires data to operate the defined models (block 630). In one embodiment, the system 100 acquires data from the computer system 130 in order to operate the defined models. The system 100 then populates the defined models with the data acquired by the system 100 for operation of the models (block 640). In other words, the system 100 sends operation data, control parameter data, simulation data, and the like, to the defined models so that the defined models can perform a simulation ***as if an actual manufacturing process were being performed***. The completion of the steps described in FIG. 6 substantially completes the step of preparing process models for simulation, as indicated in block 510 of FIG. 5.

With regard to the first emphasized section above, that section states that "the process control environment 180 can receive data from the manufacturing environment 170," there is no indication that the received data is data for setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool. The received data may well have been metrology data, which would have been data taken on a sample sent to the metrology tool 150.

Indeed, Sonderman et al specifically call out at col. 4, line 67, to col. 5, line 9, that the manufacturing environment 170 can send metrology data results into the simulation environment 210, and further state:

> The simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide more accurate, modified control parameters to the process control environment 180. A feedback loop in then completed when the process control environment 180 sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers.

Metrology data would be of no consequence to initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

With regard to the second emphasized section, the examiner will note that the description there is consistent with the statistical multi-variant description in Sonderman et al of their device model, discussed above, which also would be of no consequence to initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

Thus, these passages relied on by the Examiner fail to disclose any indication of any process data being used to set initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

Accordingly, Sonderman et al fail to disclose setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool.

Secondly, the combination of Sonderman et al and Jain et al is improper because it is without a reasonable expectation of success and a person skilled in the art at the time of the invention would not have been motivated to risk control of a semiconductor processing unit to the unproven technology of Jain et al's MPE.

The examiner has relied in the past on Jain et al for an asserted teaching of solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model. As previously noted, Jain et al describe at pages 372-373 that:

> We ***propose*** a wafer scale implementation of the MPE. The starting point would be a dedicated processing cell, optimized specifically for the PDE arithmetic and data routing. Because of the relative simplicity of the cell, it is expected that extremely large arrays (8x8 to 32x32) ***could be*** successfully processed on a single piece of silicon using Wafer Scale Integration techniques. In fact, we have already laid the foundation for the development of such a processing cell. Our Universal Multiply-Subtract-Add [11] ***could be*** adapted for this first cell design. Similarly, our nonlinear coprocessor cell [12]-[14] ***might be used*** in conjunction with the UMSA to provide advanced mathematical functions. As suggested in Fig. 2, there would be ***courtyards of processors***, each with two interconnection networks and two memory banks. 2-D, 3-D, and 4-D problems could then be mapped for parallel computations. Since inter-processor delays are very small (say a few ns), extremely high speeds could be achieved. This, together with the high degree of parallelism,

> would result also in high throughout. We ***envision*** 100 to 1000 processors (on one wafer) forming a wafer scale MPE. At a clock frequency of 50 MHz, a single wafer could achieve up to 20 GFLOPs performance. With our nonlinear coprocessor added, each instruction could equate to multiple floating point operations.
>
> Furthermore, because of the extendible architecture, several wafers ***could be*** interconnected as shown in Fig. 5 to construct a "stacked" MPE wafer system (SMPE). Note that no vertical interconnects within the stack of wafers are expected. Tens to hundreds of GFLOPs performance in a volume the size of a desk-top computer [15] ***could*** thus be achieved. However, ***these predictions*** ignore the likely technical advances in the next five years; a tenfold further increase in performance ***might be achievable***. [Emphasis Added]

Thus, as emphasized above, the proposed development work in Jain et al requires the development of ***futuristic*** computational equipment which one of ordinary skill in the art would be reluctant to implement or utilize for the rigorous standards needed in semiconductor manufacturing.

Yet, the prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Court in *Medichem S. A. v. Rolabo S. L.*, 437 F3d 1157, 77 USPQ2d 1865 (Fed. Cir. 2006) explained that:

> As stated above, an obviousness determination requires not only the existence of a motivation to combine elements from different prior art references, but also that a skilled artisan would have perceived a reasonable expectation of success in making the invention via that combination. While the definition of "reasonable expectation" is somewhat vague, our case law makes clear that it does not require a certainty of success. See In re O'Farrell, 853 F.2d 894, 903-04 (Fed. Cir. 1988) ("Obviousness does not require absolute predictability of success. . . . [A]ll that is required is a reasonable expectation of success.").
>
> However, to have a reasonable expectation of success, one must be motivated to do more than merely to "vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful." Id. at 903. ***Similarly, prior art fails to provide the requisite "reasonable expectation" of success where it teaches merely to pursue a "general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it.***" Id. [Emphasis added.]

Here, Jain et al merely teach to pursue a general approach that seems to be a promising field of experimentation (i.e., the future obtainment of a sophisticated Mathematical Physical Engine MPE).

As attested to in the declaration filed in related application U.S. Serial No. 10/673,507, with the computing capability of Jain et al representing **futuristic, unrealized capability,** there is no reasonable expectation of success that computer-encoded differential equations of a first principles simulation model for a spatially resolved model of a semiconductor processing tool could have been solved in a time frame shorter in time than the actual process being performed in the semiconductor processing tool.

Accordingly, a person skilled in the art at the time of the invention would **not** have been motivated to risk control of a semiconductor processing unit to the unproven technology of Jain et al's MPE. Furthermore, a person skilled in the art at the time of the invention would **not** have had available to him Jain et al's MPE to use in a first principles simulation.

Hence, for these reasons, a combination of Sonderman et al and Jain et al is **not** proper.

Thirdly, Tan et al do not teach solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed.

The examiner in related application U.S. Serial No. 10/673,507 relied on Tan et al for their teaching of at col. 2, lines 7-10, of model-based real time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run. Yet, a "model-based" real time process control does **not** specify when the model is completed, only that the "process control" in Tan is real time and does not

indicate that a solution to computer-encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool can be obtained in a time frame shorter in time than the actual process being performed

Accordingly, Applicants resubmit that Tan et al do not disclose solving computer-encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool in a time frame shorter in time than the actual process being performed.

Tan et al teach the use of an ***existing*** process model for feedback or feed forward processing. In feedback control, by definition, the results of a process step are provided to a subsequent wafer. In the feed forward control of Tan et al, the results of a prior process step are used to adjust a subsequent process being run of the wafer. Tan et al describe:

> The illustrative APC Framework 200 includes a process model 202 that receives ***feed-forward and feed-back data*** and calculates a processing parameter. The illustrative portion of the APC Framework 200 includes two measurement devices, in particular a pre-process metrology machine 204 and a post-processing metrology machine 206. The pre-process metrology machine 204 performs a measurement on a material prior to processing in a processing machine 208 and sends the measurement, as feed-forward data, to the process model 202. The processing machine 208 sends processed material to the post-processing metrology machine 206 ***to measure post-process data which is sent to the process model 202 as feedback data***.
>
> Referring to FIG. 4, a schematic block diagram shows material flow of a processing step 400 of a semiconductor manufacturing process from a process engineer perspective. An APC plan 402 ***retrieves a process model*** from the data store 306, then executes a parameter calculation algorithm 404. The APC plan 402 gives the calculated parameters to a machine 406 and directs the machine 406 to execute the process. The machine 406 issues a signal to the APC plan 402 ***when the process execution is complete***. The APC plan 402 sends the calculated parameters to the data history store 310 of the historical database 312.
>
> Referring to FIG. 5, a schematic block diagram shows material flow of a post-process measurement step 500 of a semiconductor manufacturing process from a process engineer perspective. An APC plan 502 sends a message to a machine 504 instructing the machine 504 to measure a post-processed material. The machine 504 sends measurement data to the APC

> plan 502. The APC plan 502 retrieves an old process model from the data store 306. The APC plan 502 executes a model update algorithm 506. The APC plan 502 ***stores an updated model in the data store 306 for usage in the processing step 400***. The APC plan 502 sends new model data to the data history store 310 of the historical database 312. [Emphasis added.]

Thus, Tan et al use post-process data to ***update and store*** a model for ***a subsequent processing step***. It is the **updated** model (completed ahead of the next run) that is used to control the next process run, thereby providing the model-based real time process control during the process run.

In other words, in Tan et al, the solution to the model exists ***prior to process control is not derived concurrently with the process control.***

Figure 2 of Tan et al (reproduced below) shows explicitly the use of "feed-forward data" and "feed-back data" for process control modifications. Figure 3 of Tan et al shows explicitly the use of "pre-process metrology" in what would be a feed-forward control scheme. Figures 4 and 5 describe the use of an updated model to control a subsequent process.

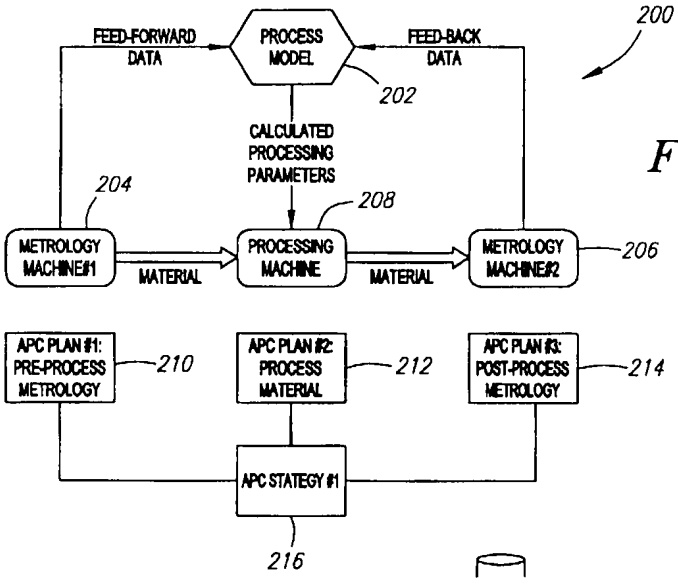


FIG. 2

Figures 6-24 of Tan et al provide implementation details as to the processing described above.

Moreover, the previously filed declaration noted above attested to the fact that neither Sonderman et al nor Tan et al use a first principles simulation model. Rather, **as attested to**, the models in these references are 1) simplified models based on former approximate solutions or 2) statistical or "learned" models tracking how the systems are expected to behave.

Thus, even if the reading of the whole of Tan et al is discredited by the examiner, then the claim's recitation of ***solving computer-encoded differential equations of the first principles simulation model*** for a spatially resolved model of a physical geometry of the semiconductor processing tool is still **not** met because Tan et al do not use a first principles simulation model. In fact, as noted above, only Applicants have realized that computer-encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool can be solved in a time frame shorter in time than the actual process being performed.

Recent guidelines from the Patent Office regarding *KSR* published in Federal Register vol. 75, No. 169 (September 1, 2010) indicates at section five (5):

> 5. Federal Circuit Cases Discussing Consideration of Evidence. ***Office personnel should consider all rebuttal evidence*** that is timely presented by the applicants when reevaluating any obviousness determination. In the case of a claim rendered obvious by a combination of prior art references, applicants may submit evidence or argument to demonstrate that the results of the claimed combination were ***unexpected***.
>
> Another area that has thus far remained consistent with pre- *KSR* precedent is the consideration of rebuttal evidence and secondary considerations in the determination of obviousness. As reflected in the MPEP, such evidence should not be considered simply for its "knockdown" value; rather, all evidence must be reweighed to determine whether the claims are nonobvious.
>
> Once the applicant has presented rebuttal evidence, Office personnel should reconsider any initial obviousness determination in view of the entire record. *See, e.g., In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788*

> *(Fed. Cir. 1984); In re Eli Lilly & Co., 90 F.2d 943, 945, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990).* All the rejections of record and proposed rejections and their bases should be reviewed to confirm their continued viability.
>
> MPEP § 2141.
> Office personnel should not evaluate rebuttal evidence for its "knockdown" value against the *prima facie* case, *Piasecki, 745 F.2d at 1473, 223 USPQ at 788,* or summarily dismiss it as not compelling or insufficient. If the evidence is deemed insufficient to rebut the *prima facie* case of obviousness, Office personnel should specifically set forth the facts and reasoning that justify this conclusion.

In *Ex parte Malone*, the Board reversed an obviousness decision reached by the examiner who had not considered the proffered evidence. *Ex parte Malone* stated:

> The Examiner's response to Nykerk Declaration is largely dismissive. In fact, even though Appellants' Briefs place extensive reliance on the Nykerk Declaration to overcome the prima facie case, the Examiner's Answer never addresses it in any detail. This is improper. Whether the claimed invention would have been obvious cannot be determined without considering evidence attempting to rebut the prima facie case. Manifestly, the Examiner's consideration and treatment of the Nykerk declaration is improper, since the Examiner has not reweighed the entire merits of the matter. Rather, he has dismissed the evidence of nonobviousness in a cursory manner. Since the Examiner did not properly consider the submitted evidence, the rejection cannot be sustained.

Support for Applicants' position on this matter is also found in the following three references, previously supplied ***as rebuttal evidence***:

1) U.S. Pat. No. 6,185,472;
2) U.S. Pat. No. 7,047,095; and
3) U.S. Pat. No. 6,587,744.

The first reference describes a simulator that can be used "proceding semiconductor manufacturing processes" or for "correcting" predetermined schedules "without using testpieces." See col. 5, line 11-21. In other words, the simulator simulates process conditions and predicts outcomes based on the simulation such that optimized process recipes can then be used. In this aspect, U.S. Pat. No. 6,185,472 is similar to Tan et al.

The improvements in ab intio calculations described in U.S. Pat. No. 6,185,472 allow a "prediction" of new process pathways by which semiconductor materials can be processed ***(i.e., in future runs)***. Column 74 of U.S. Pat. No. 6,185,472 shows a reduction in processing time from 15900 minutes to 159 minutes for the ab initio simulations. This timeframe of ***over 2 hours*** for one simulation is too long and unworkable for real time process simulation and control.

The second and third references describe feedback and feed forward process control where the result of a simulation would not be obtained during the performance of the actual process to control the actual process being performed, and therefore would not be used to control the actual process performed by the semiconductor processing tool. In this aspect, U.S. Pat. No. 7,047,095 and U.S. Pat. No. 6,587,744 are similar to Tan et al.

The second reference describes in the Summary Section:

> In the system achieved in the first aspect or in the method achieved in the second aspect, the control device may engage the transfer apparatus to transfer the workpieces at least having undergone the processing executed by the processing apparatus to the measuring apparatus, compare a measurement value indicating the results of the processing having been executed on a workpiece which is obtained through the measuring operation executed by the measuring apparatus on the workpieces at least having undergone the processing, with a target value for the processing results, and reset the processing conditions for the processing apparatus in correspondence to an error in the measurement value relative to the target value if the error is judged to be equal to or greater than a specific value. It is to be noted that the measuring operation may be executed on the workpiece before and after undergoing the processing, instead of executing the measuring operation only on the workpiece having undergone the processing.
>
> The workpiece at least having undergone the processing executed by the processing apparatus may be transferred by the transfer apparatus to the measuring apparatus which then executes a measuring operation on the workpiece at least having undergone the processing. The control device may compare a measurement value indicating the results of the processing having been executed on the workpiece obtained based upon the results of the measuring operation by the measuring apparatus with a target value for the processing results, observe the state of the fluctuation of an error in the measurement value relative to the target value so as to predict the tendency of the fluctuation and adjust the processing conditions for the processing

> apparatus in correspondence to the tendency of the fluctuation error before the error exceeds a predetermined value. It is to be noted that in this case, too, the measuring operation may be executed on the workpiece before and after the processing instead of executing the measuring operation only on the workpiece having undergone the processing.

The third reference describes in the Abstract:

> A[n] automated run-to-run controller for controlling manufacturing processes comprises set of processing tools, a set of metrology tools for taking metrology measurements from the processing tools, and a supervising station for managing and controlling the processing tools. The supervising station comprises an interface for receiving metrology data from the metrology tools and a number of variable parameter tables, one for each of the processing tools, collectively associated with a manufacturing process recipe. The supervising station also includes one or more internal models which relate received metrology data to one or more variables for a processing tool, and which can modify variables stored in the variable parameter table to control the process tools using feedback and/or feed-forward control algorithms. Feed-forward control algorithms may, in certain embodiments, be used to adjust process targets for closed loop feedback control. The supervising station may have a user interface by which different feedback or feed-forward model formats (single or multi-variate) may be interactively selected based upon experimental or predicted behavior of the system, and may also permit users to utilize their own models for run-to-run control.

Thus, the only data of record with regard to a time frame for solving computer-encoded differential equations of a first principles simulation model is that given above of ***over 2 hours***.

The Office has provided **no** evidence of any solution times **prior to the invention** for the solving of computer-encoded differential equations of a first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool.

Fourthly, in support of Applicants' position on the non-obviousness of the claims, the filed declaration in related application U.S. Serial No. 10/673,507 attested to the fact that, prior to the filing of this application, a two-dimensional axisymmetric time-evolution temperature simulation of a chuck with a wafer, a plasma heat load, and a coolant heat removal was performed. By setting initial and boundary conditions ***to values appropriate for***

the physical chuck setup, a time-evolving solution was obtained in less than 5 seconds, for a process of nominal duration of 60 seconds.

The model result expedited by the two-dimensional axisymmetric simplifications and the setting of initial and boundary conditions to values appropriate for the physical chuck setup.

The declaration attested to the fact that this simulation time gave a 12:1 factor time compression available for altering the controls to prevent running into "out-of-spec" process conditions, based on the prediction. This simulation result ***in less than 5 seconds*** occurred with all temperatures initialized to 0 deg C.

The declaration attested to the fact that, if an actual temperature at each time step from a previous wafer run had been used for initialization, the solver would not have had to make that many equilibrium iterations on each time step, even further shortening the time of solution.

As explained in the declaration in related application U.S. Serial No. 10/673,507, this result utilized a single core PC, with 1 GB of RAM (~2002), using ANSYS general-purpose simulation code, without any parallelization, and represented at the time ***an unexpected result***.

Hence, for all of these reasons given above, Claims 1-7, 9-11, 14-34, 36-38, 41-54 and 58-60 should be found non-obvious and passed to allowance.

Conclusion:

In view of the present amendment and in light of the above discussions, the application as amended herewith is believed to be in condition for allowance.

Respectfully submitted,

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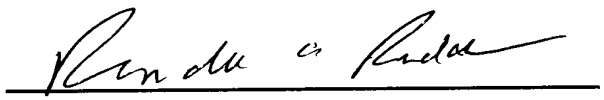

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